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Docket No. 20661-801USD1

#5/4-502  
J.D.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:  
Varun Singh et al.

Serial No.: 09/964,192

Filed: September 26, 2001

Examiner: E. Lee

Confirmation No.: 2113

For: AN IMPROVED POLYSILICON RESISTOR HAVING ADJUSTABLE  
TEMPERATURE COEFFICIENTS AND THE METHOD OF MAKING THE SAME

BOX: NON-FEE AMENDMENT  
Assistant Commissioner for Patents  
Washington, D.C. 20231

CERTIFICATE OF MAILING	
I hereby certify that this correspondence is being deposited postage paid with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231	
on	3-6-02
Signature	Joy L. Mowery

**RESPONSE TO RESTRICTION REQUIREMENT**

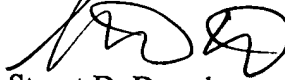
Sir:

Responsive to the communication dated January 31, 2002, requiring Applicants to elect between Claims 1, 2, 11 and 12 drawn to a semiconductor device and Claims 3-10 and 13-15 drawn to a method of making a semiconductor device, Applicants hereby elect without traverse Claims 1, 2, 11 and 12 drawn to semiconductor device and respectfully request the examination of these claims at this time. Applicants withdraw from consideration Claims 3-10 and 13-15.

Applicants respectfully request the thorough consideration of this application and earnestly solicit an early notice of allowance.

Respectfully submitted,

JENKENS & GILCHRIST,  
A Professional Corporation



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